
**Workshop Organized by:**
**Giovanni De Micheli** (*EPFL*) and **Heinrich Meyr** (*Visiting Professor, EPFL*)

The continuing pursuit of "**Moore's Law**" in semiconductor industry for more than 40 years is presenting increasingly more significant challenges for high-complexity systems and products, including:

- Unsustainable power dissipation
- Near-atomic scale dimensions - physical limits
- Increasing process and device variability
- Diminishing performance increase with scaling
- Lack of appropriate design tools and environments
- Excessive R&D and manufacturing costs

"**More Moore**" activities aim to improve CMOS performance for the 22nm node technology and beyond. The outcomes should be applicable both in pushing forward highly scaled devices and as technology boosters that allow longer life to existing geometries.

This workshop views the design of ultra-complex system-on-chip from different angles. Three distinguished speakers from industry will present their views.

**22 March 2013, EPFL, Room MXF1**

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| 8:45-9:00 | **Coffee & Croissants** |
| 9:00-9:05 | **Opening remarks** |
| 9:05-9:45 | **Designing Analog/Mixed-Signal IP Beyond the 28nm Process Technology Node**<br>**Joachim Kunkel**<br>*Synopsys Inc., California, USA* |
| 9:45 – 10:00 | **Q & A Session** |
| 10:00-10:40 | **Trends and Challenges in Wireless SOC Design**<br>**Michael Speth**<br>*Intel, Germany* |
| 10:40-11:00 | **Q & A Session** |
| 11:00-11:40 | **More Moore: Does It Mean Mixed-Signal Integration or Disintegration?**<br>**Ravi Subramanian**<br>*Berkeley Design Automation, California, USA* |
| 11:40-12:00 | **Q & A Session** |
| 12:00-12:30 | **Panel Discussion** |

http://si.epfl.ch/MoreMoore